IN THE SPECIFICATION

Please amend the paragraph beginning at page 6, line 25 as follows:

High boost signal source 64 is embodied in a primary current mirror 150 operating with a secondary current mirror ~~152~~ 154. Low boost signal source 66 is embodied in primary current mirror 150 operating with a secondary current mirror 154.

Please amend the paragraph beginning at page 9, line 6 as follows:

High boost signal source 74 is embodied in a primary current mirror 250 operating with a secondary current mirror ~~252~~. Low boost signal source 76 is embodied in primary current mirror 250 operating with a secondary current mirror ~~254~~.

Please amend the paragraph beginning at page 9, line 9 as follows:

Primary current mirror 250 includes a diode-coupled transistor 260 in series with a transistor 262 between a signal input locus 265 and an upper voltage supply line 238 maintained substantially at an upper supply voltage V_{CC}. A boost current reference signal I_{BSTREF} is applied at signal input locus 265. Boost signal I_{BSTREF} establishes the boost signal level for effecting data indications in write head 52. Current mirror ~~200~~ further includes a diode connected transistor 264 coupled in series with transistors 266, 268 between lower voltage supply line 208 and upper voltage supply line 238 via a transistor 269. Preferably transistors 260, 264, 266 are bipolar transistors and transistors 262, 268, 269 are metal oxide silicon (MOS) transistors. Transistors 262, 268 are gated by bias signal V_{REF2}. Bias signal V_{REF1} gates transistor 269 so that boost signal I_{BSTREF} is permitted to flow through transistors 264, 266, 268, 269. Transistors 260, 262, 266, 268 cooperate to mirror boost signal I_{BSTREF} (biased toward upper voltage signal V_{CC}) to flow through transistors 270, 272 when transistor 272 is

gated to conduct. Transistor 264 cooperates with transistors 260, 262, 266, 268 cooperate to mirror boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) to flow through transistors 274, 276 when transistor 276 is gated to conduct. Transistor 276 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTLX2 to gate locus ~~217~~ via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 274, 276 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52. Transistor 272 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTHX2 to gate locus 273 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 270, 272 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52.